



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/596,035

03/20/2007

Konrad Bach

D4695-00152

1923

8933 7590 03/17/2008

DUANE MORRIS, LLP
IP DEPARTMENT
30 SOUTH 17TH STREET
PHILADELPHIA, PA 19103-4196

EXAMINER

YAM, STEPHEN K

ART UNIT

PAPER NUMBER

2878

MAIL DATE

DELIVERY MODE

03/17/2008

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/596,035	Applicant(s) BACH ET AL.	
	Examiner STEPHEN YAM	Art Unit 2878	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-19 is/are rejected.
- 7) ☒ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 20 March 2007 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. ____. |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>20061106</u> . | 6) <input type="checkbox"/> Other: ____. |

DETAILED ACTION

Claim Objections

1. Claim 10 is objected to because of the following informalities:

In Claim 10, line 6, “the buried photocell portion” lacks proper antecedent basis

In Claim 10, line 7, “the chip” and “the chip front side” lack proper antecedent basis.

In Claim 10, line 11, “the backside” lacks proper antecedent basis.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 1, the phrase "(chip normal)" renders the claim indefinite because it is unclear whether the limitations following the phrase are part of the claimed invention. See MPEP § 2173.05(d).

Regarding claim 2, the phrase "(specifically)" renders the claim indefinite because it is unclear whether the limitations following the phrase are part of the claimed invention. See MPEP § 2173.05(d).

Art Unit: 2878

Regarding claim 2, the phrase "in particular" renders the claim indefinite because it is unclear whether the limitations following the phrase are part of the claimed invention. See MPEP § 2173.05(d).

Regarding Claim 3, "said filled trenches" and "the crystalline semiconductor" lack proper antecedent basis when the claim is dependent on claim 1 - for examination purposes, Examiner will interpret Claim 3 as depending on Claim 2 only.

Regarding claim 3, the phrase "particularly" renders the claim indefinite because it is unclear whether the limitations following the phrase are part of the claimed invention. See MPEP § 2173.05(d).

Regarding claim 3, the phrase "(conductively)" renders the claim indefinite because it is unclear whether the limitations following the phrase are part of the claimed invention. See MPEP § 2173.05(d). "

Regarding Claim 4, "filled trenches" is already defined when the claim is dependent on claim 2.

Regarding claim 5, the phrase "(insulation)" renders the claim indefinite because it is unclear whether the limitations following the phrase are part of the claimed invention. See MPEP § 2173.05(d).

Regarding claim 7, the phrase "in particular" renders the claim indefinite because it is unclear whether the limitations following the phrase are part of the claimed invention. See MPEP § 2173.05(d).

Art Unit: 2878

Regarding claim 7, the phrase "(standard)" renders the claim indefinite because it is unclear whether the limitations following the phrase are part of the claimed invention. See MPEP § 2173.05(d).

Regarding claim 8, the phrases "(detector side)" and "(chip on lead)" render the claim indefinite because it is unclear whether the limitations following the phrase are part of the claimed invention. See MPEP § 2173.05(d).

Regarding claim 9, the phrase "(chip carrier stripe)" renders the claim indefinite because it is unclear whether the limitations following the phrase are part of the claimed invention. See MPEP § 2173.05(d).

Regarding claim 10, it is unclear what elements (amplifier, evaluation electronics, photocell portion) is included as formed in the common single crystalline semiconductor material. For examination purposes, Examiner interprets all the elements as formed in the semiconductor material.

Regarding claim 15, the phrase "(insulation)" renders the claim indefinite because it is unclear whether the limitations following the phrase are part of the claimed invention. See MPEP § 2173.05(d).

Regarding claim 17, the phrase "preferably" renders the claim indefinite because it is unclear whether the limitations following the phrase are part of the claimed invention. See MPEP § 2173.05(d).

Regarding claim 17, the phrases "(carrying the evaluation electronics in a later stage)", "(chip carrier stripe)", "(the side carrying said electronic circuit)" renders the claim indefinite

Art Unit: 2878

because it is unclear whether the limitations following the phrase are part of the claimed invention. See MPEP § 2173.05(d).

Regarding Claim 18, it is unclear whether the claim is referring to an order of performing method steps and what the "continuous numbering" refers to- the claim should refer to the numerals (eg., 17.1, 17.2, ...) of the method steps for improved clarity.

Claims 6, 11-14, 16, and 19 are indefinite by virtue of their dependency on an indefinite claim.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Myrosznyk US Patent No. 5,365,088 in view of Lindemann et al. US Patent No. 6,919,609.

Regarding Claim 1, Myrosznyk teaches (see Fig. 1) a photodetector for processing low luminous intensities comprising a transimpedance amplifier (14) (see Col. 4, lines 15-20) and evaluation electronics (multiplexing circuits- see Col. 4, lines 15-20), further comprising an actual photocell portion (12) is associated with one chip side (top of (16)), from which preferably light is incident (see Fig. 1), an electronic circuit portion (14) formed on the opposite chip side; electric connections (18) between said photocell portion and the electronic circuit portion, said electric connections extending in a direction (vertical) parallel to an orthogonal direction with

Art Unit: 2878

respect to the chip plane (see Fig. 1). Myrosznyk does not teach the transimpedance amplifier as monolithically integrated. Lindemann et al. teach (see Fig. 1) a similar device with a monolithically integrated transimpedance amplifier (see Col. 2, lines 27-33). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the transimpedance amplifier as monolithically integrated, as taught by Lindemann et al., in the device of Myrosznyk, to provide improved manufacturing of the device and integration of the amplifier into the device.

Allowable Subject Matter

6. Claims 10-16 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, and claim objections, set forth in this Office action.

7. Claims 2-9 and 17-19 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter:

Regarding Claim 2, the invention as claimed, specifically in combination with a monolithically integrated transimpedance amplifier and evaluation electronics, with the electric connections between the photocell portion and the electronic circuit portion formed by specifically filled trenches doped in specified areas that are extending in a crystalline semiconductor, is not disclosed or made obvious by the prior art of record.

Regarding Claim 4, the invention as claimed, specifically in combination with filled trenches filled with doped polysilicon for establishing the electric connections between the photocell portion and the electronic circuit, is not disclosed or made obvious by the prior art of record.

Regarding Claim 10, the invention as claimed, specifically in combination with monolithically integrated transimpedance amplifiers and evaluation electronics and a buried photodiode portion formed on a common single crystalline semiconductor material, with the buried photocell portion and overlying electronic circuit portions associated with a chip front side, electronic connections provided as trenches between the buried photocell portion and the electronic circuit portion, with the electric connections extending in a direction of the chip normal or a parallel direction, wherein light to be detected is received from a chip backside, is not disclosed or made obvious by the prior art of record.

Regarding Claims 7 and 17, the invention as claimed, specifically in combination with a monolithically integrated transimpedance amplifier and evaluation electronics, and using high-ohmic silicon, forming an area of opposite conductivity type by counter-doping based on a mask and subsequently annealing the wafer side, performing an epitaxy process, contacting the counter-doped layer by means of a Sinkers diffusion or specifically filled trench, planarizing at least the trenches, performing a CMOS or BiCMOS process for forming the integrated electronic circuit on one wafer side, thinning the wafer at the other side, forming an antireflective coating above said one side, and separating and mounting the chips and sealing the chips with a sealing material, is not disclosed or made obvious by the prior art of record.

Art Unit: 2878

Regarding Claim 17, the invention as claimed, specifically in combination with a monolithically integrated transimpedance amplifier and evaluation electronics, and using high-ohmic silicon, forming an area of opposite conductivity type by counter-doping based on a mask and subsequently annealing the wafer side, performing an epitaxy process, contacting the counter-doped layer with a Sinkers diffusion or specifically filled trench, planarizing at least the trenches, performing a CMOS or BiCMOS process for forming the integrated electronic circuit on one wafer side, thinning the wafer at the other side, forming an antireflective coating above said one side, and separating and mounting the chips and sealing the chips with a sealing material, is not disclosed or made obvious by the prior art of record.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Fenk US 4,314,152, Spartiotis US 6,188,089, Spartiotis et al. US 7,189,071, and Spartiotis et al. US 6,323,475 teach similar devices but do not disclose or make obvious the claim limitations recited above in the reasons for allowance.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to STEPHEN YAM whose telephone number is (571)272-2449. The examiner can normally be reached on Monday-Friday 8:30am-5pm.

Art Unit: 2878

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Georgia Epps can be reached on (571)272-2328. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Stephen Yam/
Primary Examiner, Art Unit 2878